LOW POWER CSD LINEAR PHASE FIR FILTER ARCHITECTURE USING VIRTUAL COMMON SUBEXPRESSION AND FILTER DESIGN METHOD THEREFOR

ABSTRACT OF THE DISCLOSURE

An apparatus and method for digital filtering includes a method for implementing a digital filter having filter coefficients, each expressible as a canonical signed digit code word; where the method includes forming a virtual common subexpression that is relevant to a first filter coefficient, forming a second subexpression for a second filter coefficient in terms of the virtual common subexpression so that adders are shared with the virtual common subexpression in a tap line of the second filter coefficients; and the resulting digital filter receives digital samples of input signals, shifts the received digital samples by bit-shift values of filter coefficients that are defined relative to the virtual common subexpression, adds shifted digital samples to drive a common tap line, adds shifted digital samples to the output of the common tap line to drive a tap line corresponding to a filter coefficient, and delays an output signal component corresponding to a tap line.